

EAST - [thinsearch12.wsp.1]

File View Edit Tools Window Help

☒ L1: (4) "6096644"  
☒ L2: (3) "6162691"  
☒ L3: (6) "6130102"  
☒ L4: (3) "6072221"  
☒ L5: (219356) semiconductor and (contact plug)  
☒ L6: (12750) L5 and interlayer  
☒ L7: (16123) L5 and silicide  
☒ L8: (3102) L6 and silicide  
☒ L9: (6520) L7 and hole  
☒ L10: (2162) L8 and hole  
☒ L11: (608) L10 and insulator  
☒ L12: (125) L11 and self-aligned

☐ Failed  
☒ Saved  
☒ (5985) (diode and recovery) and switching

Search:      
 DBs: USPAT; US-PGPUB; EPD; JPD; DERWENT; IBM TDB  
 Default operator:  ☐ Plurals ☐ Synonyms  
☒ Highlight all hit terms initially

L11 and self-aligned

☒ BRS form ☒ IS&R form ☐ Image ☐ Text

	U	1	Documen	Issue	Pag	Title	Curr	Current	Re	Inventor
1	<input type="checkbox"/>	<input type="checkbox"/>	US		29	Semiconductor integrated circuit manufacturing met				Tsuchiaki, Masakatsu
2	<input type="checkbox"/>	<input type="checkbox"/>	US		60	Semiconductor integrated circuit device and process				Yamada, Satoru Oyu, Kiyonori Ikeda, Shuji
3	<input type="checkbox"/>	<input type="checkbox"/>	US		69	Semiconductor integrated circuit device				Meguro, Satoshi Segawa, Mizuki
4	<input type="checkbox"/>	<input type="checkbox"/>	US		15	Semiconductor device and method for fabricatin				Uehara, Takashi Adachi, Hirocki
5	<input type="checkbox"/>	<input type="checkbox"/>	US		22	Semiconductor device and method for manufact				Takenouchi, Akira

Start     EAST - [thinsearch1... EAST Browser - L12: (125) 7:01 PM

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File View Edit Tools Window Help

☐ Pending

☒ Active

- ☒ L1: (7) "6096595"
- ☒ L2: (1) L1 and ( molybdenum or tantalum )
- ☒ L3: (2381) molybdenum adj silicide
- ☒ L4: (22) L3 and (contact adj plug )
- ☒ L5: (22) L4 and layer
- ☒ L6: (8) L5 and ( tantalum adj silicide)
- ☒ L7: (2) (contact adj plug )and (silicide adj pad)
- ☒ L8: (20) silicide adj pad
- ☒ L9: (4) "6265779"

Search List Browse Queue Clear

DBs: USPAT: US-PGPUB: EPO: JPO: DERWENT: IBM TDB

Default operator: OR

☐ Plurals ☐ Synonyms

☒ Highlight all hit terms initially

L11 and self

BRS form IS&R form Image Text

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6335247 B1	20020101	10	Integrated circuit vertical trench device and method of forming thereof	438/270	438/268 : 438/733
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6284633 B1	20010904	7	Method for forming a tensile plasma enhanced nitride capping layer over a	438/585	438/153 : 438/592
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6137132 A	20001024	11	High density buried bit line flash EEPROM memory cell with a shallow	257/315	257/314
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6038164 A	20000314	19	SRAM cell configuration and method for its fabrication	365/154	257/385 : 365/180
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5578508 A	19961126	9	Vertical power MOSFET and process of fabricating the same	438/270	438/289 : 438/302
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5416736 A	19950516	19	Vertical field-effect transistor and a semiconductor memory cell having	365/174	257/380 : 257/381
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5364810 A	19941115	19	Methods of forming a vertical field-effect transistor and a	438/153	438/156 : 438/302

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File View Edit Tools Window Help

BRS: L4 and mask

Pending

Active

- L1: (8) "5641991"
- L2: (1529) multilayer adj interconnect
- L4: (202) multi-layer adj interconnect
- L5: (1702) L2 or L4
- L6: (951) polysilicon adj plug
- L7: (40) L5 and self-aligned
- L8: (21160) self adj aligned
- L9: (43) L8 and L5

Search List Browse Queue Clear

DBs: USPAT: US-PGPUB: EPO: JPO: DERWENT: IBM TDB

Plurals Synonyms

Default operator: OR

Highlight all hit terms initially

L8 and L5

BRS form IS&R form Image Text

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20020014673 A1		95	Method of making membrane integrated circuits		
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20010029081 A1		15	Method for producing semiconductor device		
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6294909 B1	20010925	90	Electro-magnetic lithographic alignment method	324/207.17	324/226 : 324/262
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6197681 B1	20010306	11	Forming copper interconnects in dielectric materials with low constant	438/637	438/624 : 438/627
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6025244 A	20000215	13	Self-aligned patterns by chemical-mechanical polishing particu	438/386	438/243
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6020257 A	20000201	88	Membrane dielectric isolation IC fabrication	438/626	438/630
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6008126 A	19991228	88	Membrane dielectric isolation IC fabrication	438/667	438/668
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5998251 A	19991207	18	Process and structure for embedded DRAM	438/241	438/253

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